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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/340,172	06/25/99	WON	D

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EXAMINER	
COLEMAN, E	
ART UNIT	**PAPER NUMBER**
2183	2

DATE MAILED: 09/20/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/340,172	Applicant(s) WON, DEREK CHI-LAN	
	Examiner Eric Coleman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24 and 27-43* is/are rejected.

7)☒ Claim(s) *25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5,12,16-17,20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond (patent No. 5,638,525).

Hammond taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) instruction transformation unit(741) (e.g., see fig. 7) that transforms code from one instruction set architecture to a transformed instruction set architecture (e.g., see col. 2, lines 32-67);

b) instruction cache which transmits a stream of data (e.g., see figs. 3,4,5,6,7);

Hammond did not expressly detail (claim 1) that the transformation unit transformed instructions in units of blocks. Hammond however taught the instructions stored in a cache memory. It was well known in the DP art to store instructions in a cache in units of blocks. Consequently it would have been obvious to one of ordinary skill in the DP art that the instructions that were retrieved from the cache for translation in the Hammond system would have been retrieved and translated in blocks.

Hammond taught (claim 2) direct execution of the original and translated instruction set architectures (e.g., see col. 1, lines 60-67, and col. 2, lines 53-67). As to

the limitations of claims 3,4,12,20,and 21, Hammond taught (e.g., see col. 12, lines 41-67) use of the x86 instruction set which is known to comprise in order and out of order (i.e., superscalar) processing capabilities which include reordering instructions.

As to the limitation of claim 5 Hammond taught (e.g., see fig. 5) working memory connected to the instruction stream transformation unit.

As to the limitations of claims 16-17, Hammond taught the use of RISC instructions (e. g, see col. 44-66). Register windowing is conventionally used with RISC processors.

Claims 6-11,13,22-24,27,32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond as applied to claims 1-5,12,16,17,20-21, above, and further in view of Farber (patent No 6,105,124).

Farber taught transformation of instructions in units of hyperblocks (e.g., see fig. 1 and col. 2, line 58- col. 3, line 24 and col. 4, lines 30-61) with tags indicating the start of the block (e. g, see fig. 1) and using a block identifying name (e.g., see col. 4, lines 47-67) . As to the if-predication transformation Farber taught decoding each instruction into opcode and operand and transforming each instruction into target instructions (e.g., see col. 4, lines 8-33). If-then instructions were well known conditional instructions. Therefore it would have been obvious to one of ordinary skill that the If predication transformation would have occurred in the Farber system.

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Hammond and Faber. The use of of hyperblocks provide for more efficient locating of the translated branching instructions and therefore incorporaton of the Faber

teachings including the hyperblocks would have enabled more efficient retrieval of translated instructions in the Hammond system (e.g., see col. 1, lines 28-62 of Faber).

Claims 14,15,18,19,28,29,30,31,33-38,40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ireton (patent No. 5,826,089).

Ireton taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) instruction transformation unit(14) (e.g., see fig. 1) that transform code from one instruction set architecture to a transformed instruction set architecture (e.g., see col. 2, lines 34-67);

b) instruction cache (12)which transmits a stream of data (e.g., see figs. 1,2).

Ireton did not expressly detail (claim 1) that the transformation unit transformed instructions in units of blocks. Ireton however taught instructions stored in a cache memory. It was well known in the DP art to store instructions in a cache in units of blocks. Consequently it would have been obvious to one of ordinary skill in the DP art that the instructions that were retrieved from the cache for translation in the Ireton system would have been retrieved and translated in blocks.

Ireton taught (claim 14) speculative execution of instructions (e.g., see col. 5, lines 2-17). Therefore since a load instruction is an instruction that was required by a conventional processor such as the Ireton system then it would have been obvious to one of ordinary skill that the Ireton would have comprised some type of load that was speculatively executed and translated.

Ireton also taught dependency checking (claims 15,18,19,30,31)(e.g., see col. 6, lines 4-16). As to the limitations of claims 40-42, the dependency matrix was not specified but the tabular storing of data In a DP system was well known and this would have been recognized by one of ordinary skill to provide efficient retrieval of specific dependency data. Also, the use of dependency pointers or vectors was not detailed but the use of pointers would have been obvious to one of ordinary skill in the art.

Ireton did not expressly detail (claim 38) using physical registers that have not been commited to hold results and allowing a final instruction in the group to commit the physical register results to a logical register. However in the superscalar implementation of the Ireton teaching it would have been obvious to one of ordinary skill that a physical register would have not been committed being it is was used to hold results and likewise the final instruction in a group would have commited register results to a logical register during processing.

As to the limitations of claims 33-37 Ireton taught scheduling of processing (e.g., see col. 5, lines 1-24). Ireton also taught branch prediction with speculative fetching if a branch is mispredicted (e.g., see col. 5, lines 5-17) and counters for counting the decoded instructions (e.g., see col. 7, lines 10-50). Therefore although the claimed history tables were not specified the use of branching history tables for branch prediction was well known in the DP art at the time of the claimed invention. Also with the number of counters used in the Ireton system it would have been obvious to one of ordinary skill in the DP art that the Ireton system would have comprised history tables for storing the run-time behavior of the system to improve scheduling of the instructions.

Claims 39,43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faber (patent No. 6,105,124).

Faber taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Means and method for assigning a sequence number to the the original instruction set architecture instruction starting from the beginning of the block (e., see fig. 1);

b) Means and method for marking each of the transformed instruction set architecture instruction with the corresponding instruction sequence number (e.g., see fig. 1 and col. 2, lines 25-67).

Faber did not expressly detail (claim 39) committing the results in order of the sequence numbers. Faber however taught the system was related to systems which used conventional instruction sets such as x86 instructions (e.g, see col. 1,lines 20-27) In these conventional instruction set computers the results are commited in order. Therefore it would have been obvious to one of ordinary skill in the DP art that the results in the Faber system would have been committed in the order of the sequence number assigned to the data locations.

Also although Faber did not specifically detail (claim 43) that the tranformation processing was done in software It would have been obvious to one of ordinary skill that in at least one implementation of the Faber teachings the transformation processing was done in software.

Allowable Subject Matter

Claims 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shiell (patent No. 5,913,049) disclosed a mult-stream complex instruction set microprocessor (e.g., see fig. 1,and abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-9051 for regular communications and (703) 308-9052 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-3900.

ERIC COLEMAN
PRIMARY EXAMINER

EC
September 19, 2001